PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|
| re Application of: Keisuke GOTO, et al. | : | |
| ppl. No.: 09/826,179 | : | Art Unit: 2816 |
| Filed: April 4, 2001 | : | Examiner: LE, Dinh Thanh |
| For: **DLL CIRCUIT AND METHOD OF GENERATING TIMING SIGNALS** | : | Atty Docket: KPM-01501 |

## DECLARATION OF KEISUKE GOTO UNDER 37 CFR 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. I, Keisuke Goto, am an originally named inventor of U.S. Patent Application Serial No. 09/826,179, filed in the United States on April 4, 2001, (hereinafter "the U.S. patent application) which claims priority to Japanese Patent Application No. 2000-103241, filed on April 5, 2000 (hereinafter "the Japanese patent application").

2. Prior to April 3, 2000, I, in collaboration with the other inventor, conceived of the invention described and claimed in the Japanese patent application and in the U.S. patent application and disclosed the invention to a Japanese patent attorney firm for preparation of a specification for a patent application.

3. Subsequent to the disclosure to the Japanese patent attorney firm but prior to April 3, 2000, the Japanese patent attorney firm transmitted a draft patent application to me for review.

4. Attached hereto as Exhibit A is a Japanese language facsimile cover sheet reflecting the transmission to me of the draft patent application. The dates of this document have been redacted. However, all of the redacted dates are prior to April 3, 2000.

5. Attached hereto as Exhibit B is an English language translation of the facsimile cover sheet of Exhibit A.

6. Attached hereto as Exhibit C is an English language translation of the draft patent application transmitted to me with the facsimile cover sheet of Exhibit A.

7. Exhibit C fully supports all of the features of the invention described and claimed in the Japanese patent application and currently claimed in the U.S. patent application. (See, for example, pages 3 - 6 of Exhibit C.)

8. From the date of transmission of the draft patent application until the filing date of April 5, 2000, the Japanese patent attorney firm and I worked together diligently on the patent application to prepare it for filing with the Japanese Patent Office.

9. All of the work that is reflected in the Japanese patent application was performed in Japan, a WTO country.

10. As indicated by the foregoing statements and the attached Exhibits, there was reasonable diligence in working to constructively reduce the invention to practice from a time prior to April 3, 2000, until the invention was constructively reduced to practice by filing the Japanese patent application on April 5, 2000.

11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title XVII of the United States Code and that such willful false statements may jeopardize the validity of this Application for Patent or any patent issuing thereon.

Respectfully submitted,

Date: 2004/2/2

Keisuke Goto

Keisuke GOTO

(原紙)

1/25


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## Facsimile

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弊所担当者 ：山下 晴朗
発明者 ：五藤 敬介 様
発明の名称 ：ＤＬＬ回路、半導体装置、ＤＬＬ回路の遅延方法、及び、半導体装置の動作方法

総数 ：送信原稿はこの頁を含めて ２５枚です。

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送信物件

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|---|---|---|
| 願書 | ： | １頁 |
| 明細書 | ： | １４頁 |
| 図面 | ： | ８頁 |
| 要約書 | ： | １頁 |

以上

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**Exhibit B**
(Translation of Exhibit A)



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Date: Fax No. 044-435-1871
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Client ID.: 74410380
(Concurrent application hantoku-tokusyutu-0914)
Our ID.: 12JPDP977
Person in charge: Haruo YAMASHITA
Inventor: Keisuke GOTO
Title of the Invention: DDL CIRCUIT, SEMICONDUCTOR DEVICE, DELAYING METHOD IN DLL CIRCUIT, AND OPERATION METHOD OF SEMICONDUCTOR DEVICE

Sheets: 25 sheets including this sheet

(Omitted)

**Exhibit C**



# VERIFICATION OF TRANSLATION

I, Minoru KUDOH
of a citizen of Japan residing at: 406, 17-15,
Minamiooi 1-chome, Shinagawa-ku, Tokyo 140, Japan
declare that I am well acquainted with the Japanese and English languages and that, to the best of my knowledge, ability and belief, the attached translation of a draft of the Japanese Patent Application document No. 2000-103241 is a true and faithful translation of that document.

This 5 day of January, 2004

Minoru KUDOH

[Document Name] PATENT APPLICATION
[Identification No.] 74410380
[Filing date]
[To] Commissioner of Japanese Patent Office
[International Patent Classification] H03L 7/00

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[Indication of Charge]
[Deposit Payment Register Number] 053213
[Amount of Fee] 21000yen
[Items of the Filing Articles]

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|---|---|---|
| [Article Name] | Specification | one copy |
| [Article Name] | Drawings | one copy |
| [Article Name] | Abstract | one copy |

[General Power of Attorney] 9715177

[Document Name] Specification

[Title of the invention]

DDL CIRCUIT, SEMICONDUCTOR DEVICE, DELAYING METHOD IN DLL CIRCUIT, AND OPERATION METHOD OF SEMICONDUCTOR DEVICE

[Scope of Patent to be Claimed]

[Claim 1] A DDL circuit comprising:

a variable delay circuit in which a delay time depends on a frequency;

a phase control circuit which controls said delay time of said variable delay circuit based on a phase difference between an input side signal of said variable delay circuit and an output side signal of said variable delay circuit;

a fixed delay circuit which is connected to an output side of said variable delay circuit and in which a delay time does not depend on a frequency, wherein said fixed delay circuit includes a delay element; and

a signal line connected to a node between said delay element and said variable delay circuit to take out a delayed signal.

[Claim 2] The DDL circuit according to claim 1, wherein said input side signal corresponds to an external clock signal, and

said output side signal corresponds to an internal clock signal.

[Claim 3] The DDL circuit according to claim 2, wherein said internal clock signal includes a first internal clock signal and a second internal clock signal, and

said first internal clock signal is said output side signal, and said second internal clock signal is said delayed signal.

[Claim 4] The DDL circuit according to claim 1, wherein said output side signal is an output signal of said fixed delay circuit.

[Claim 5] The DDL circuit according to claim 1, wherein said delay element includes delay element components serially connected in multiple stages, and

said node is between said delay element component in a final stage of said delay element components, which component is the farthest from said variable delay circuit, and said variable delay circuit.

[Claim 6] The DDL circuit according to claim 1, wherein said delay element includes a plurality of delay element components serially connected in a multiple-stage, and

said node is between said delay element component in a final stage, which is the farthest from said variable delay circuit in said delay element components, and a delayed element component, which is nearer to said variable delay circuit than said delay element component of final stage in said plurality of delay element component.

[Claim 7] The DDL circuit according to claim 6, wherein said plurality of delay element components are inverters, and said delay element component, which is nearer to said variable delay circuit than said delay element component of final stage in said plurality of delay element components, is an inverter which is nearer to said variable delay circuit in even number stage than said delay element component of the final stage in said plurality of delay element components.

[Claim 8] The DDL circuit according to claim 1, wherein a delay time of said delayed signal is shorter than a half of half cycle of said output side signal.

[Claim 9] The DDL circuit according to claim 1, wherein a cycle of said output side signal is shorter than 5 ns and the delay time is less than 10% of said cycle.

[Claim 10] A semiconductor device which is controlled by a DDL circuit described in Claim 1, includes a memory circuit, wherein said delayed signal is used as an operation signal to operate said memory circuit.

[Claim 11] The semiconductor device according to Claim 10, wherein said input side signal is a signal corresponding to an external clock signal,

said output side signal is a signal corresponding to an internal clock signal,

said internal clock signal includes a first internal clock signal and a second internal clock signal,

said first internal clock signal is said output side signal, said second internal clock signal is said delayed signal, and

said first and second internal clock signals are used as an operation signal to operate said memory circuit.

[Claim 12] The semiconductor device according to Claim 10, wherein said delay element includes delay element components connected in series in a multiple-stage, and

said node is between a delay element component of the final stage, which is in the farthest from said variable delay circuit in said delay element components, and said variable delayed circuit.

[Claim 13] The semiconductor device according to Claim 10, wherein said delay element includes delay element components connected in series in a multiple-stage, and

said node is between said delay element component of the final stage, which is in the farthest from said variable delay circuit in said delay element components, and a delay element component, which is nearer to said variable delay circuit than said a delay element component of final stage in said plurality of delay element component.

[Claim 14] The semiconductor device according to Claim 10, wherein a delay time of said delayed signal is shorter than a half of half cycle of said output side signal.

[Claim 15] The semiconductor device according to Claim 10, wherein a cycle of said output side signal is shorter than 5 ns and the delay time is less than 10% of said cycle.

[Claim 16] A delay method in a DDL circuit comprising the steps of:

generating a first delayed signal which depends on a frequency of said basic clock signal with delaying control by feedback controlling of a phase of basic clock signal;

generating a second delayed signal which does not depend on a frequency of said basic signal from said first delayed signal; and

generating a third delayed signal which does not depend on a frequency of said basic signal from said first delayed signal,

wherein, said third delayed signal is a signal in the process of generating said second delayed signal.

[Claim 17] An operation method of a semiconductor device, which control an operation of a semiconductor device by a delay method of a DDL circuit described in Claim 16, including a step of generating a signal to operate said semiconductor device based on said third delayed signal.

[Claim 18] The operation method of semiconductor device according to Claim 17 including a step of switching a read operation and a write operation of memory based on said operation signal, wherein said switching is carried out during a half cycle of said basic clock signal.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention belongs]

The present invention relates to a DDL circuit, a semiconductor device, a delay method in the DDL circuit, and an operation method of the semiconductor device. Especially, the DDL circuit, the semiconductor device, the delay method in the DDL circuit, and the operation method of the semiconductor device which have no malfunction in a circuit operation such as a logic operation based on an internal clock signal which does not depend on a frequency of an external clock signal to be used.

[0002]

[Conventional Technique]

A synchronization establishment is needed to speed up the operation of semiconductor devices. An internal clock signal is used for the synchronization. The internal clock signal is generated on the basis of an external clock. The phase of the internal clock signal generated thus needs to be coincident with the phase of the external clock signal or a strict definition of the relative phase difference. To coincide the phase, the DDL circuit is used. The external clock is delayed by a variable delay circuit whose delay time depends on a frequency and is variable and is outputted as the internal clock signal.

The external clock signal and the internal clock signal generated thus are compared in phase. Then, the delay time of the variable delay circuit is adjusted based on a phase control

circuit which carries out a feed back phase control based on the difference between the phases. As a result of such feedback, the phase of the internal clock signal coincides that of the external clock signal.

[0003]

Such an internal clock signal is used as an operation signal which operates a semiconductor device containing a memory, a logic circuit and a CPU. The phase of the internal clock signal, which is in phase synchronization with the external clock, is controlled to be applied to the object for the clock signal by a fixed delay circuit. The delay time of the fixed delay circuit does not depend on the frequency.

A technique of delay control is disclosed in Japanese Laid Patent Application (JP-A Heisei 11-261408) and so on. Fig. 6 shows such a delay control circuit as the well known technique which is not applied only to JP H11-261408. An external clock signal Rclk is delayed by a DLL circuit 101 to supply a latch circuit 102. The latch circuit 102 is operated in response to input of an activate signal 103. A signal 104 outputted from the latch circuit 102 is further delayed by a delay circuit 105, which is composed of a multiple-stage delay element and whose delay time is constant. A signal 106 delayed thus is used in an operational section of the semiconductor device (for example; in a memory core).

[0004]

The signal 104 is shown in Fig. 2 as the conventional example. The internal clock signal outputted from the DLL circuit 101 is described as internal clock signal (on the way of adjustment). The falling edge of the internal clock signal (on the way of adjustment) is outputted from the latch circuit 102 as the signal 104 shown at the rising edge 107. The signal 104 is further delayed by the delay circuit 105 and outputted from the delay circuit 105 as the signal 106 having a delayed rising edge 108. The delay time is indicated as t2. Fig. 3 shows a signal 104' when the frequency of the external clock signal is lower than that shown in Fig. 2. The signal 104' is further delayed by the

delay circuit 105 and outputted from the delay circuit 105 as a signal 106' having a delayed rising edge 108'. The delay time dose not depend on the frequency of the internal clock signal and is constant. Therefore, the delay time is equal to the delay time shown in Fig. 2. The phase of the rising edge 108' is earlier by the phase difference t3 to the defined phase position.

[0005]

As shown in Fig. 7, due to the phase difference t3, a read enable signal RE 109 is generated in synchronization with the external clock signal Rclk (or the internal clock signal synchronized with it) as an early read enable signal RE 109' which rises up by t3 in phase difference. For this reason, in response to the falling of the latch signal 110, Data A to be ideally latched is not latched but Data B is latched. Such malfunction tends to be occurred often, as the frequency of clock signal is higher.

[0006]

Fig. 4 shows another malfunction in the circuit operation. A signal 111 shown in the drawing as a conventional example has the possibility of malfunction of operation that a WRITE operation and a READ operation overlap as shown as the status of a memory section (a conventional example). This is because that the physical variation is present in each circuit element in the manufacturing process so that the signal 111 is out of a predetermined phase position backward and forward.

Fig. 5 shows another malfunction in circuit operation. A signal 112 shown in the drawing as a conventional example is delayed to have a rising edge as shown by a solid line. A read data 113, which is read in the READ operation indicated as the status of a memory section (a conventional example), has the possibility of malfunction of operation in which the read data 113 is earlier read by a half cycle than a read data which should be read in the read operation.

[0007]

As shown in Fig. 8, when a high speed operation of a memory is required, in which the write operation and the read operation

is switched between a falling edge and a rising edge in a half cycle of the internal clock signal 113, it is required that a rising edge 115 is made earlier by about 0.15 ns to rise at the rising edge 115 in order to start up the READ operation without a malfunction, in case of, for example, the half cycle of 1.25 ns. The clock signal frequency is changed by the user, and a system test by a manufacturer or a user is carried out at a low speed. When the above-mentioned phase difference for the earlier generation is large, the data is read out too early. Therefore, it is desired to achieve the phase delaying (preceding phase) slightly but strictly. Also, it is desired to achieve the phase delaying slightly and strictly so as to make it possible to change a kind of operation in the half cycle. Moreover, the size and scale of circuit is desired to be small.

[0008]

[Problems the Invention Tries to Solve]

An object of the present invention is to provide a DDL circuit, a semiconductor device, a delay method in the DDL circuit, and an operation method of the semiconductor device, in which a slightly and strictly preceding phase can be achieved without depending on the frequency to be used.

Another object of the present invention is to provide a DDL circuit, a semiconductor device, a delay method in the DDL circuit, and an operation method of the semiconductor device, in which the size and scale of circuit can be made small.

[0009]

[Means for Solving the Problems]

A means for solving the problems will be described bellow. The technical terms in the description have numbers and symbols with parentheses "( )". The numbers and symbols correspond to the technical term in at least one of the embodiments of the present invention, particularly they coincide with the reference numbers and symbols for the technical terms described in the drawings of the embodiment.

These numbers and symbols clarify the correspondence between the technical article in the Claims and the technical article in

the embodiment. These correspondences do not mean that the technical articles in the claims are interpreted with the limitation to the technical articles in the embodiments.

[0010]

A DDL circuit of the present invention comprises: a variable delay circuit (5) in which a delay time depends on the a frequency, a phase control circuit (7) which controls said delay time of said variable delay circuit (5) based on a phase difference between an input side signal (4, 22) of the variable delay circuit (5) and an output side signal (8, 11, or 21) of the variable delay circuit 5, a fixed delay circuit (9) which does not depend on a frequency, wherein the variable delay circuit (5) is connected to an output side of the variable delay circuit(5), wherein the fixed delay circuit (9) includes delay elements (9-1 to 9-3), and a signal line connected to a node between said delay element (9-1 to 9-3) and said variable delay circuit (5) to take out a delayed signal (12).

[0011]

The delayed signal (12) outputted from an element (9-1) of the middle of the fixed delayed circuit (9) is delayed by a slight time from the delayed signal (11) outputted the fixed delayed circuit (9). The delay time is remarkably shorter in the phase length than a half cycle of the basic clock signal (4). Thus, the signal (12) which is slightly delayed in extreme precision is used as an internal clock signal as operation signal.

[0012]

An input side signal (4) corresponds to an external clock signal, and an output side signal (8 or 11) corresponds to an internal clock signal as to be used. The internal clock signal includes a first internal clock signal (11) and a second internal clock signal (12). The first internal clock signal (11) corresponds to the above-mentioned output side signal, and the second internal clock signal (12) corresponds to the above-mentioned delayed signal. In this case, the output side signal (11) corresponds to the output signal of the fixed delayed circuit (9).

[0013]

The delayed element includes delay element components (9-1 to 9-3) serially connected in multiple stages, and the above-mentioned node is between a delay element component of a final stage (9-3), which is in the farthest from the variable delay circuit (5) in the delay element components (9-1 to 9-3), and the variable delayed circuit (5). Concretely, such a node is between the delay element component of the final stage (9-3), which is in the farthest from the variable delay circuit (5) in the delay element components (9-1 to 9-3), and the delay element component (9-1), which is nearer to the variable delay circuit (5) than the a delay element component of final stage (9-3) in the plurality of delay element components (9-1 to 9-3). The plurality of delay element components (9-1 to 9-3) are preferred to be inverters. When the inverter is used as the delay element component (9-1), which is nearer to the variable delay circuit (5) than the delay element component of the final stage (9-3) in the plurality of delay element component (9-1 to 9-3), is an inverter nearer to the variable delay circuit (5) in even number stage (example 2), than the delay element component of final stage (9-3).

[0014]

It is characterized that the delay time of the delayed signal is shorter than a half of half cycle of the output side signal (basic clock signal). That is, the delay time of the delayed signal (12) is less than 10% of the cycle of the output side signal when the cycle is, for example, shorter than 5 ns.

[0015]

The semiconductor device of the present invention is controlled by such DDL circuit, and includes the memory circuit (2). The delayed signal (12) is used as operation signal to operate the memory circuit (12). Regarding the output side signal (11, 12) and the means for delaying have been already explained. Also it has been mentioned above that the delay time of the delayed signal (12) is shorter than a half of half cycle of the output side signal (11). The delay time of the delayed signal (12) is less than 10% of the cycle of the output side signal, and

it is slight and extremely precise when the cycle is shorter than 5 ns.

[0016]

A delaying method of DDL circuit of the present invention includes steps of generating a first delayed signal which depends on a frequency of the basic clock signal (4) with delaying control by feedback controlling of a phase of the basic clock signal (4), generating a second delayed signal (11) which does not depend on the frequency of the basic signal (4) from the first delayed signal (8), and generating a third delayed signal (12) which does not depend on the frequency of the basic signal (4) from the first delayed signal (8).

The third delayed signal (12) is a signal in the process of generating the second delayed signal (11).

[0017]

An operation method of semiconductor device of the present invention is the method of controlling the operation of semiconductor devices by the above-mentioned delaying method of the DDL circuit, and includes the step of generating the operating signal (15) to operate the semiconductor device by the third delayed signal (12). Then, based on the operation signal (15), a read operation and a write operation of memory are switched. Such switching is carried out precisely and strictly in a half cycle of the basic clock signal (4). It is avoidable to confuse the read operation and write operation by carrying out switching precisely in the half cycle.

[0018]

[Embodiments of the Invention]

A DDL circuit is provided together with a memory section in the embodiment of the DDL circuit of the present invention, with reference to the drawings. As shown in Fig. 1, a logic circuit 3 is provided between the DDL circuit 1 and the memory section 2. The DDL circuit 1 inputs an external clock signal 4. The well-known DDL circuit 1 (note: this portion is amended to "the DDL circuit 1 of the present invention" by the inventor) is composed of a variable delay circuit 5, a phase comparing circuit 6, a

control signal generating circuit 7 and a fixed delay circuit 9. A delay time of the variable delay circuit 5 depends on a frequency. The external clock signal 4 is supplied to the variable delay circuit 5. A delayed clock signal 8 outputted from the variable delay circuit 5 is supplied to the fixed delay circuit 9.

[0019]

A delay time of the fixed delay circuit 9 does not depend on the frequency and is peculiar to physical elements such as inverters of the fixed delay circuit 9. The fixed delay circuit 9 comprises multiple inverters 9-1, 9-2, ..., 9-n connected in series (n=3 in the drawing). The delayed clock signal outputted from the fixed delay circuit 9 is supplied to the logic circuit 3 as a first internal clock signal 11. The delayed clock signal outputted from the inverter, which is provided previously for stages of even number (in this case, 2 stages) from the inverter 9-3 at the last stage, i.e., the first inverter 9-1, is supplied to the logic circuit 3 as a second internal clock signal. The second internal clock signal 12 is preceding by 0.15 ns in phase than the first internal clock signal 11. That is, the second internal clock signal 12 is outputted from the inverter (in this example: inverter 9-1), which is provided before the inverter which outputs the first internal clock signal 11 (inverter 9-3 in this example) by the stages of even number.

[0020]

The logic circuit 3 communicates with the memory section 2 interactively based on the first internal clock signal 1 and the second internal clock signal 12 which are in synchronization with an external clock signal 4 and are delayed in phase. The contents of the communication are a write data (WD) 13, a read data (RD) 14 and a control signal 15 which controls the timing of a read operation and write operation of these data. An input signal 16, such as an instruction signal and a write data, is supplied to the logic circuit 3 through an input circuit 17. An output signal 18 such as a read data signal is outputted via an output circuit 19.

[0021]

The first internal clock signal 11 is supplied to the phase comparing circuit 6 as a feedback signal 21. The external clock signal 4 is supplied to the phase comparing circuit 6 as a basic clock signal 22. The phase comparing circuit 6 compares the phase of the feedback signal 21 and that of the basic clock signal 22, and outputs the difference between the phases as a detection signal. The phase comparing circuit 6 outputs an up signal to the phase control circuit 7 when the difference is negative and outputs a down signal to the phase control circuit 7 when the difference is positive. The phase control circuit 7 outputs a control signal 23 based on the up signal and the down signal. The variable delay circuit 5 proceeds or delays the phase of the delayed clock signal 8 on the basis of the control signal 23 so as to determine the delay time of the delayed clock signal 8 to the external clock signal 4.

[0022]

The fixed delay circuit has a multiple-stage structure in order to get a quantity of delay time. The total delay time of the inverters of an n series stages is approximately $n \cdot \Delta L$ when the delay time of the inverter at each stage is $\Delta L$. When the delay time L of the inverter of one stage is 0.15 ns/2, the clock signal outputted from the inverter 9-1 at the first stage as the second internal clock signal 12, is earlier by about 0.15 ns than the first internal clock signal 11 in phase. The respective delay times of all the inverters may be different from each other.

[0023]

Fig. 2 shows timings of the internal clock signals 11 and 12. The phase of the second internal clock signal 12 is earlier by about 0.15 ns than that of the first internal clock signal 11. A second RE signal 32 generated based on the second internal clock signal 12 is earlier by t1 in phase than a first RE signal generated based on the first internal clock signal 11. Here, the t1 is about 0.15 ns. This time t1 is a peculiar value to the inverters 9-2 and 9-3, and it does not depend on the frequency of the first and second internal clock signals 11 and 12. Therefore, it does not depend on the frequency of the external clock signal 4.

In this way, as shown in Fig. 3, the preceding time is not varied even if the frequencies of the first and second internal clock signals 11 and 12 are lowered.

[0024]

Variation of delay times in the inverters 9-1, ···, 9-n in the respective stages are considered. Then, the j-th inverter 9-j which outputs the second internal clock signal 12 is selected so as to the delay time of the second internal clock signal 12 falls within an allowable range. Once it is selected, malfunctions in the conventional circuit shown in Fig. 4 will no longer occur because of the invariability of t1. Also, in the conventional circuit in the low speed operation, the malfunction shown in Fig. 5 that data is outputted before a half cycle will not occur.

[0025]

The second internal clock signal 12 is taken out from the inverter before the stages of even number to the first internal clock signal 11. Therefore, the second internal clock signal 12 is outputted to have a preceding phase by the delay time of the inverters of the even number stages (=t1) even if the frequency is varied. Further, because the second internal clock signal 12 is a signal taken out from the DDL circuit which has low variation of electric power, the variation of the delay time by a VDD and a manufacturing process is made less.

[0026]

As shown in Fig. 2, the internal clock signal used to generate the signal 32 of the present invention, especially the edge 35 of the second internal clock signal 12 precedes in time to the internal clock signal used to generate the conventional equivalent signal 104, especially the edge 36 of the first internal clock signal 11. Therefore, the delay time of the present invention is shorter by a half cycle than that of the conventional technique, and the numbers of delay elements through which signals pass is less. The delay time is hard to be influenced on the variation of delay times, which is caused by manufacturing process and the like, in accordance with the less numbers of the delay element. It should be noted that the load of

the internal signal 12 taken out on the way of delay path, which dose not depends on the frequency of the DDL circuit, is lower than that of the final output of the DDL circuit.

[0027]

[Effect of the invention]

In the DDL circuit, the semiconductor device, the delay method in the DDL circuit, and the operation method of the semiconductor device of the present invention, a phase preceding of the operation signal is carried out without depending on the frequency, and the timing of preceding is strictly adjusted. The preceding is not influenced by a manufacturing process, and the phase difference for the preceding is slight and strict, so that the operation early for a half cycle is carried out. The DLL circuit of the present invention can help the high speed operation of the semiconductor device such as a synchronous type DRAM in which the strict timing precision is required, and allow the continuous write and read operations. Also, a pre-charge for the read operation can be started during the write operation strictly.

[Brief Description of the drawings]

[Fig. 1]

Fig. 1 is a circuit diagram showing the embodiment of the DDL circuit of the present invention.

[Fig. 2]

Fig. 2 is a timing chart showing the timing of the generation signal.

[Fig. 3]

Fig. 3 is a timing chart showing another timing of the generation signal.

[Fig. 4]

Fig. 4 is a timing chart showing further another timing of the generation signal.

[Fig. 5]

Fig. 5 is a timing chart showing further another timing of the generation signal.

[Fig. 6]

Fig. 6 is a circuit diagram showing the delay circuit which

is well known.

[Fig. 7]

Fig. 7 is a timing chart showing the operation by a publicly known signal.

[Fig. 8]

Fig. 8 is a timing chart showing the slight timing causing a malfunction.

[Description of the Reference Numerals and Symbols]

4: input side signal

5: variable delay circuit

7: phase control circuit

8, 11, 21: output side signal side

8: the first delay signal

9: fixed delay signal

9-1 to 9-3: delay inverter

11,12 delay signals

11: the first internal clock signal (the second delay signal)

12: the second internal clock signal (the third delay signal)

15: operation signal

[Document Name] Abstract

[Abstract]

[Object] To output a preceding phase signal with a slightly and strictly preceding phase without depending on a frequency.

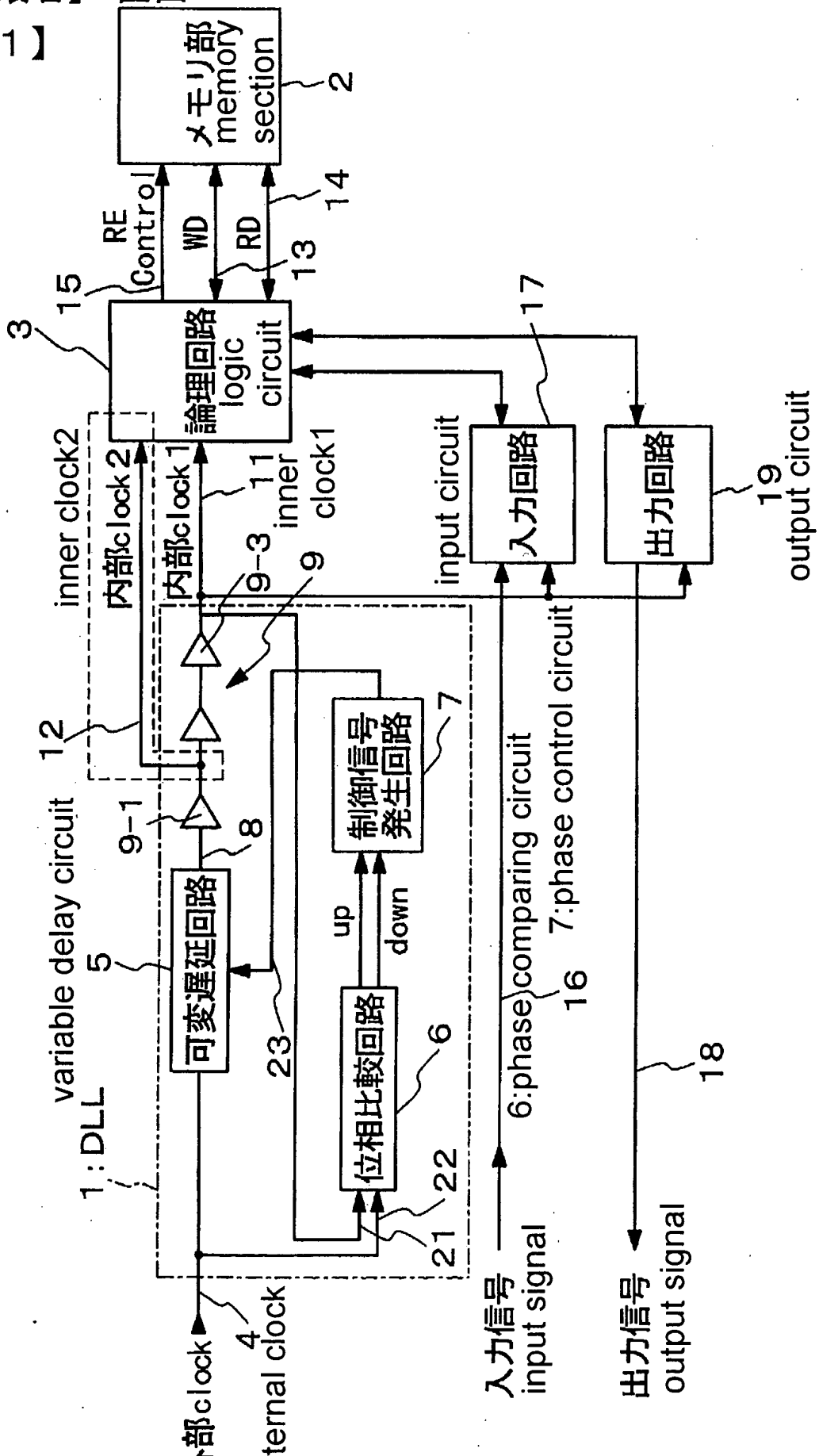
[Solving Means] A variable delay circuit 5 that a delay time depends on a frequency is provided together with a phase control circuit 7. The phase control circuit 7 controls the delay time of the variable delay circuit 5 by the phase difference of an input side signal 4, 22 of the variable delay circuit 5 and an output side signal 8, 11, 21. A fixed delay circuit 9 connected to the output side of the variable delay circuit 5 comprises delay elements 9-1 to 9-3, and a delayed signal 12 is taken out between the delay elements 9-1 to 9-3 and the variable delay circuit 5. Then, it is easy to get an internal clock signal as an operation signal which is controlled in phase slightly and strictly without depending the frequency.

[Selected Drawing] Fig. 1

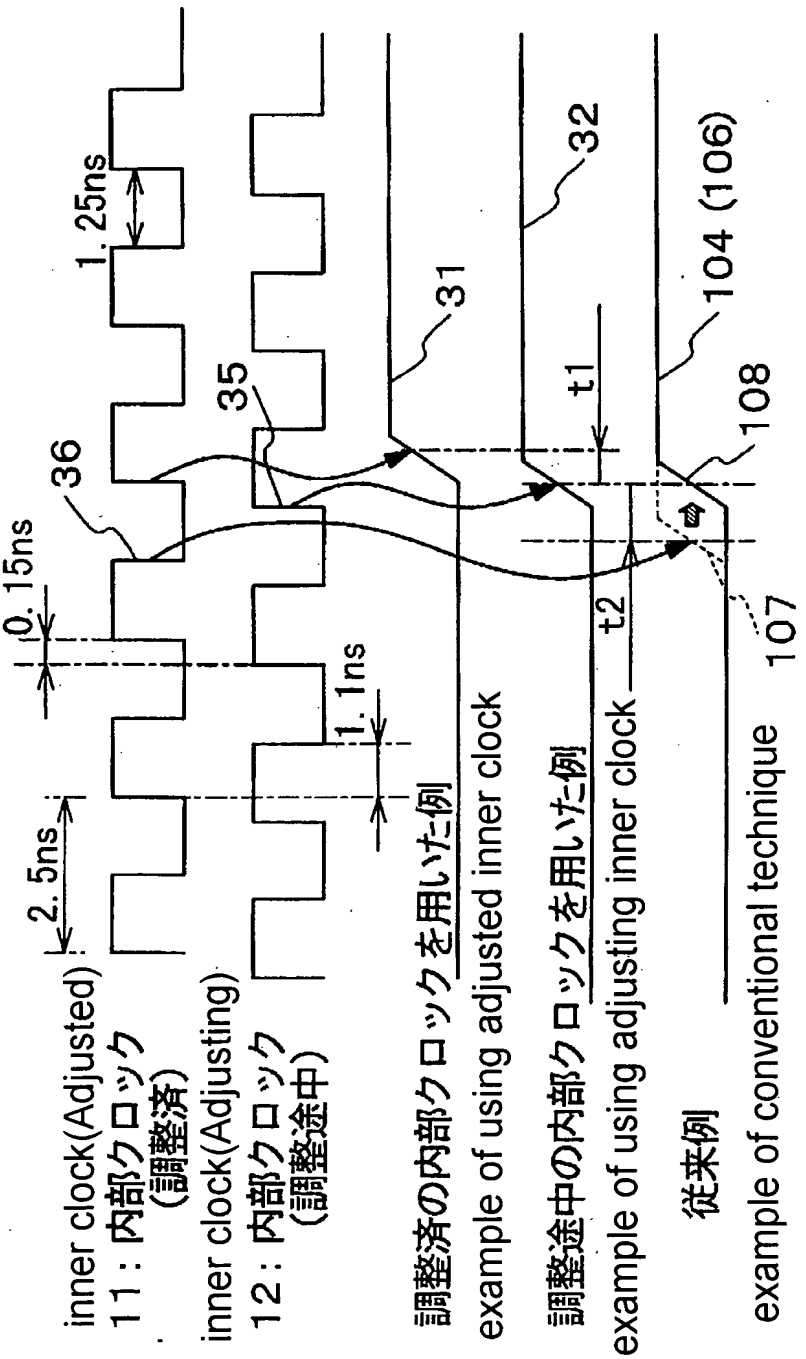
整理番号　７４４１０３８０

【書類名】　図面　　【DOCUMENT NAME】 DRAWINGS

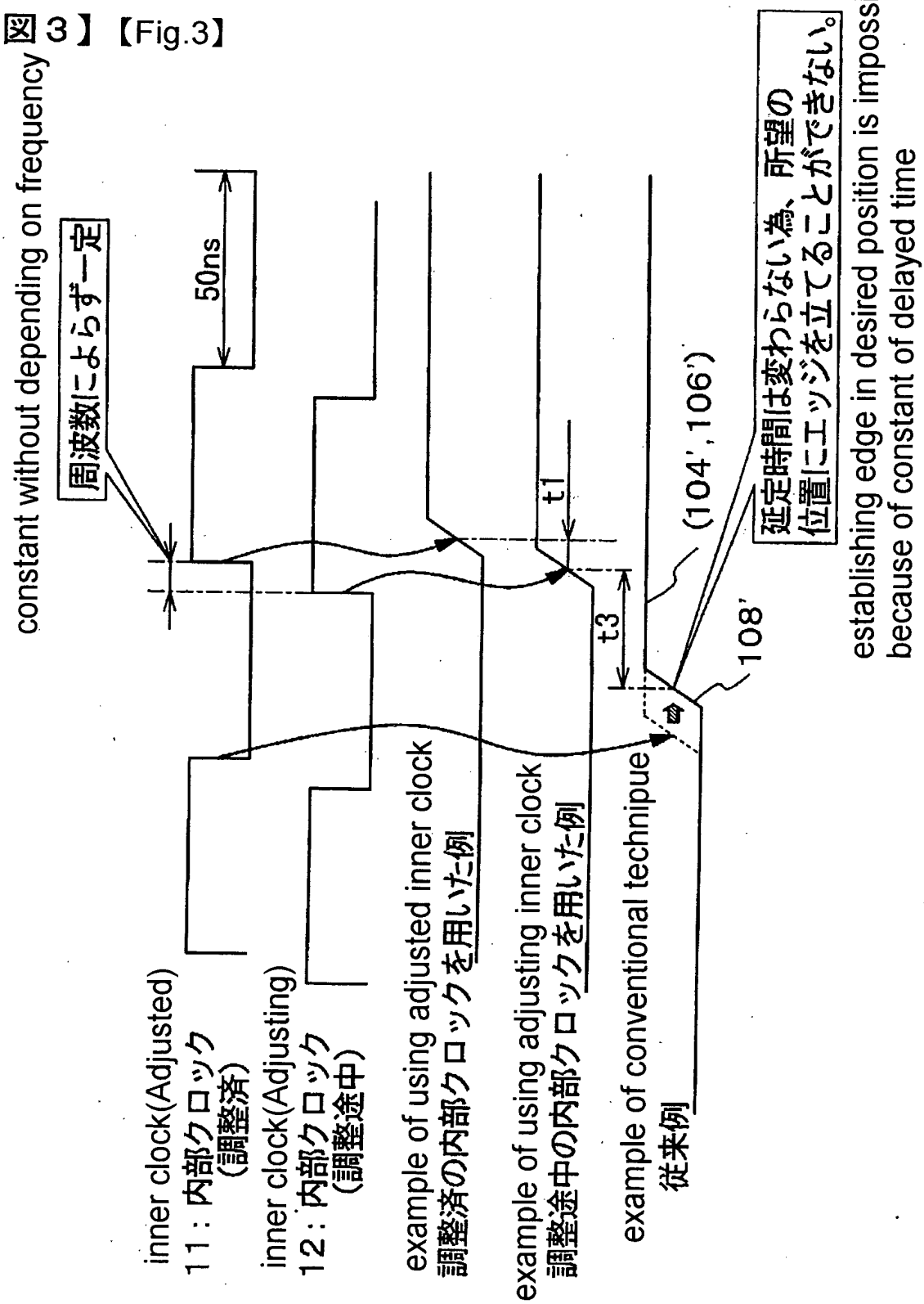
【図１】



【図２】【Fig.2】


inner clock(Adjusted)
11：内部クロック
(調整済)
inner clock(Adjusting)
12：内部クロック
(調整途中)
2.5ns
0.15ns
1.25ns
1.1ns
36
35
31
32
104 (106)
108
107
t1
t2
調整済の内部クロックを用いた例
example of using adjusted inner clock
調整途中の内部クロックを用いた例
example of using adjusting inner clock
従来例
example of conventional technique

【図３】【Fig.3】


constant without depending on frequency
周波数によらず一定
50ns
inner clock(Adjusted)
11：内部クロック
(調整済)
inner clock(Adjusting)
12：内部クロック
(調整途中)
example of using adjusted inner clock
調整済の内部クロックを用いた例
example of using adjusting inner clock
調整途中の内部クロックを用いた例
example of conventional technipue
従来例
t1
t3
(104',106')
108'
延定時間は変わらない為、所望の
位置にエッジを立てることができない。
establishing edge in desired position is impossible
because of constant of delayed time

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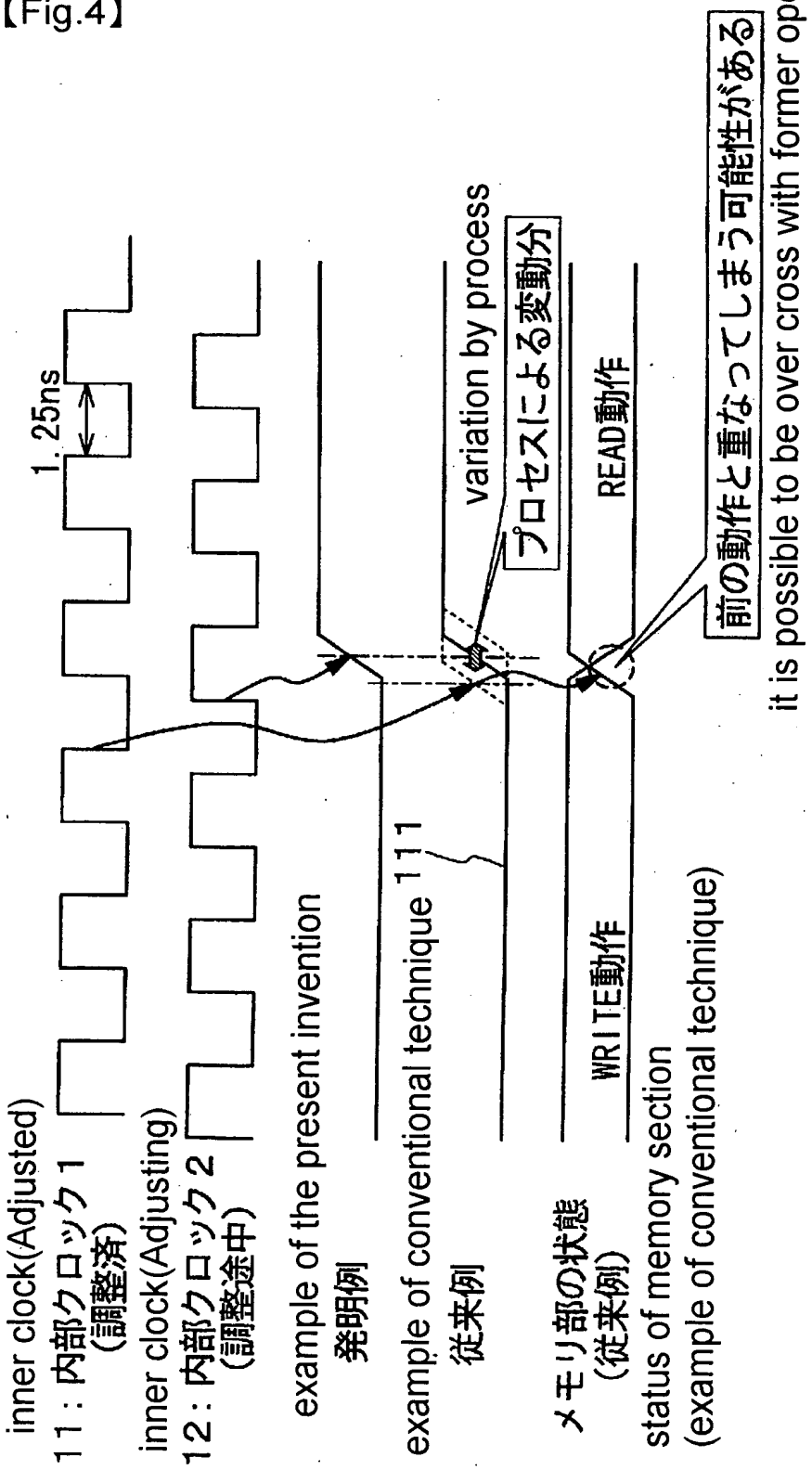
【図４】【Fig.4】



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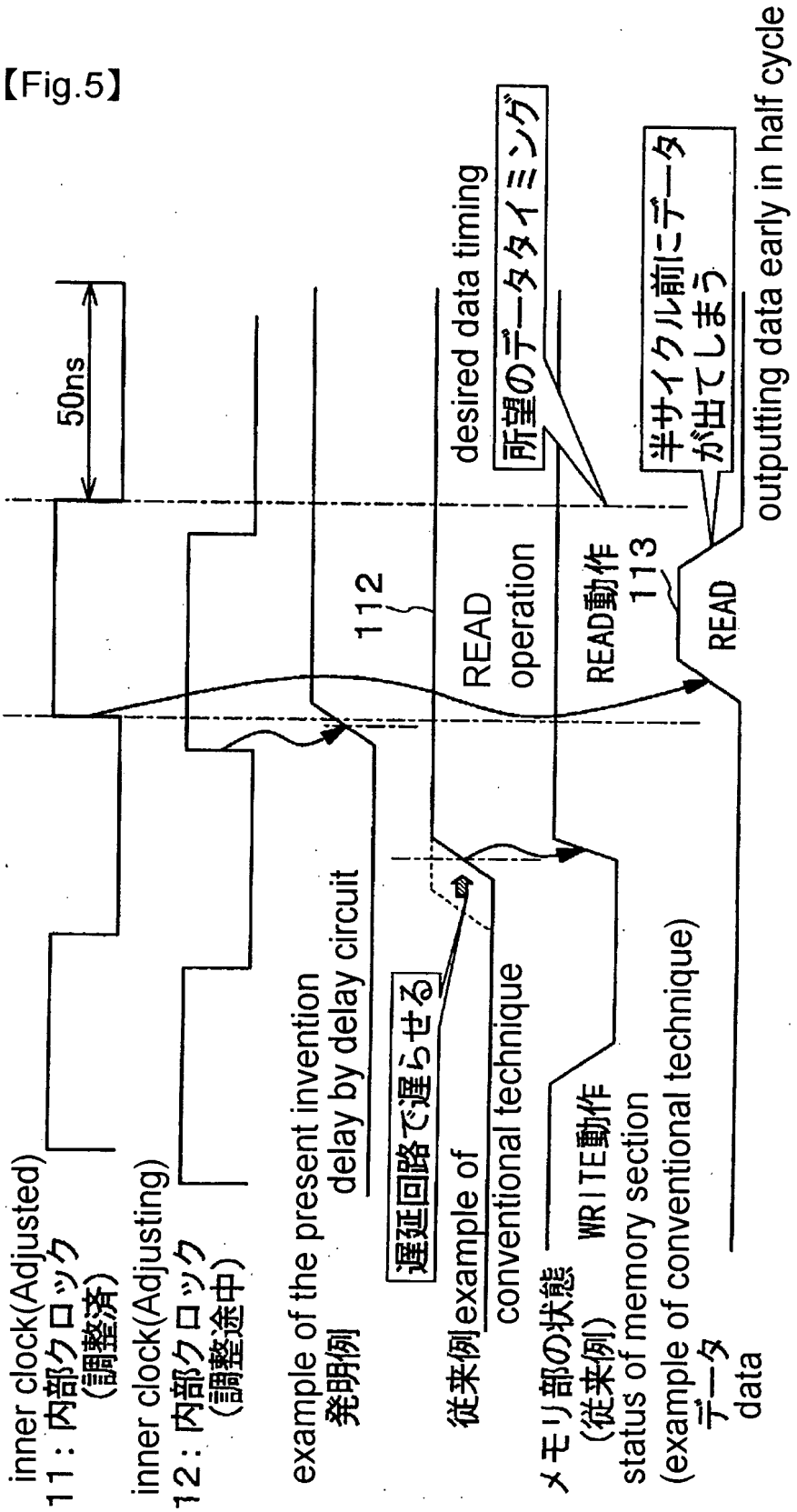
【図５】【Fig.5】



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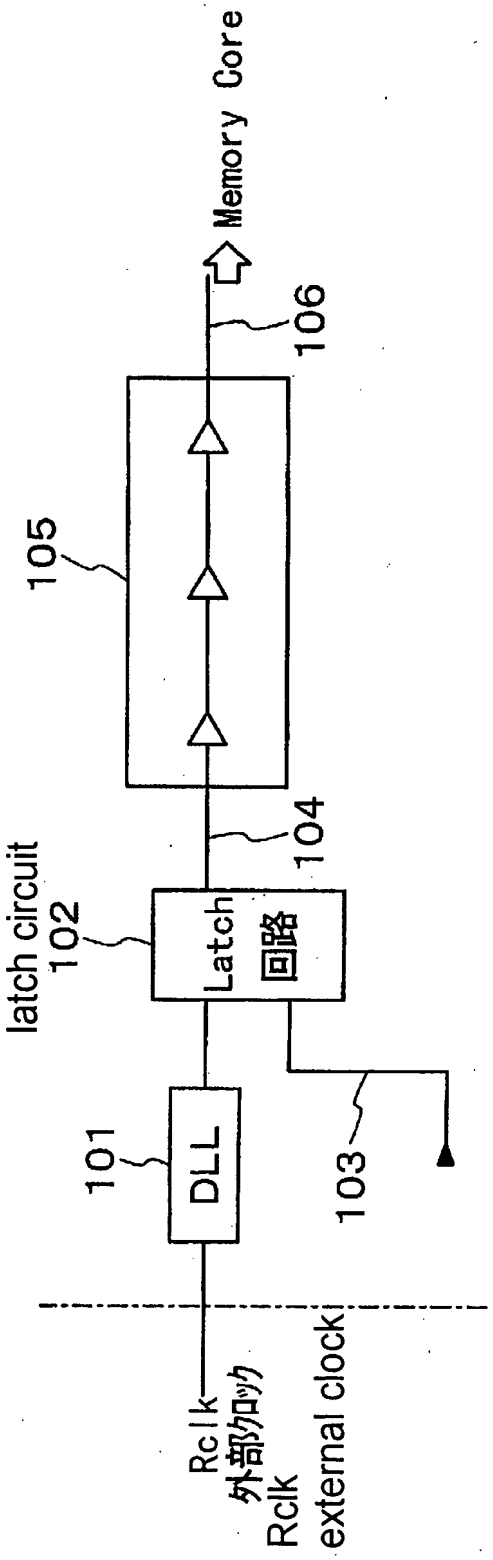
【図６】【Fig.6】



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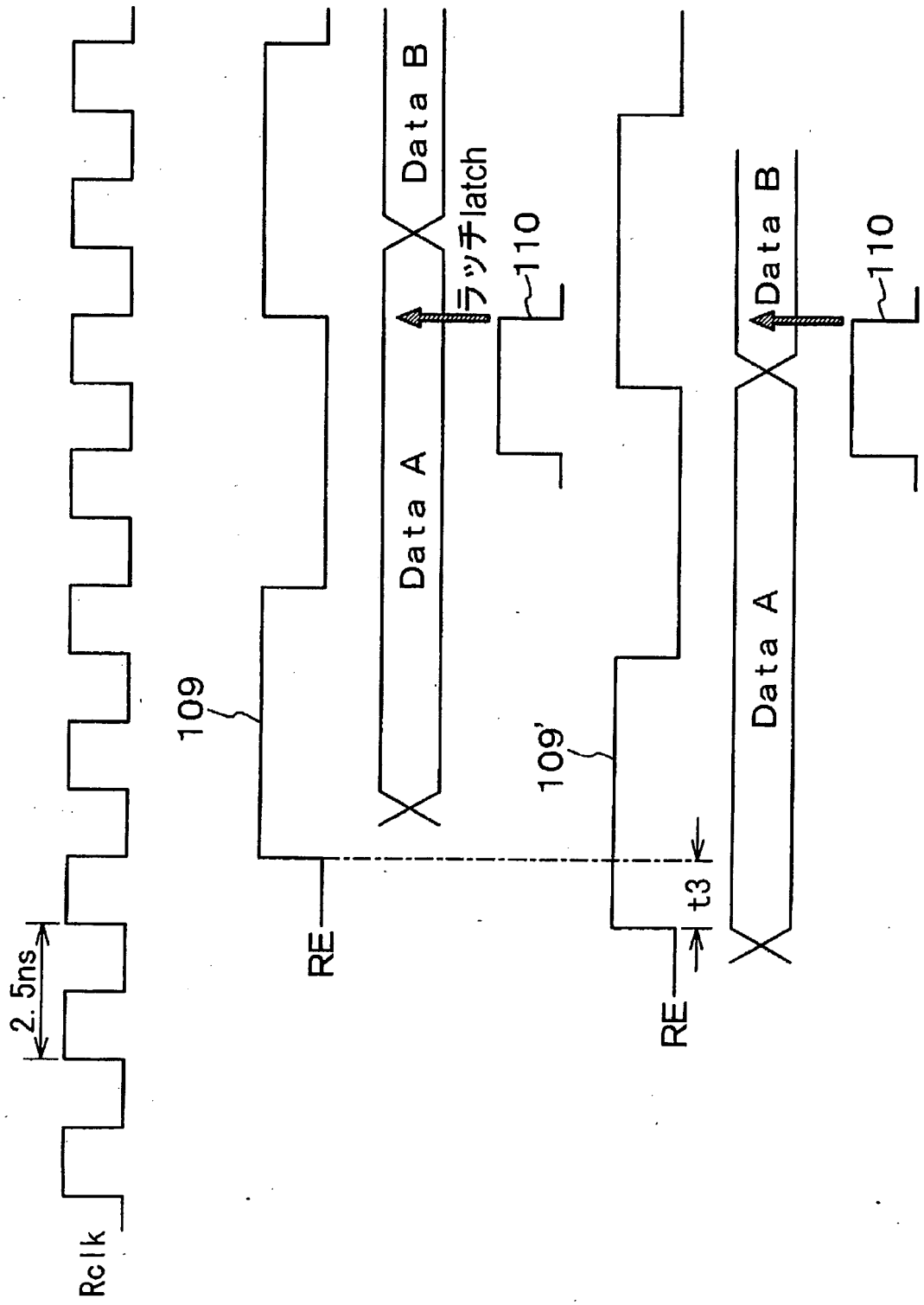
【図７】【Fig.7】



整理番号　７４４１０３８０

【図８】【Fig.8】